CLAIMS

- 1. (previously presented) A method of fabricating an integrated circuit, the method comprising: providing a substrate;
- creating at least one base-window in a layer;
- forming a monocrystalline SiGe layer in at least one region, and
- forming a polycrystalline SiGe layer elsewhere over the substrate.
- 2. (previously presented) A method as recited in claim 1, further comprising forming a polycrystalline silicon layer over selectively exposed portions of the substrate.
- 3. (previously presented) A method as recited in claim 2, further comprising forming a mask over a top surface, providing openings in selected locations of the mask, and removing the polycrystalline silicon layer to expose the selected portions of the substrate.
- 4. (previously presented) A method as recited in claim 3, wherein the exposed portions of the substrate are monocrystalline silicon.
- 5. (previously presented) A method as recited in claim 1, wherein the integrated circuit includes a lateral pnp transistor.
- 6. (previously presented) A method as recited in claim 1, wherein the integrated circuit includes an SiGe bipolar transistor.
- 7. (previously presented) A method as recited in claim 6, wherein the SiGe bipolar transistor includes the monocrystalline SiGe.
- 8. (previously presented) A method as recited in claim 1, wherein the integrated circuit includes a varactor diode.
- 9. (previously presented) A method as recited in claim 1, further comprising forming a polysilicon resistor.
- 10. (previously presented) A method as recited in claim 1, wherein only one masking step is required to form a lateral pnp transistor, varactor diode and a polysilicon resistor.

- 11. (previously presented) A method as recited in claim 10, wherein the lateral pnp transistor is a silicon device, and includes a portion of the polycrystalline SiGe layer in each of a collector contact and an emitter contact.
- 12. (previously presented) A method as recited in claim 11, wherein the polycrystalline SiGe layer is disposed beneath a polycrystalline silicon layer.
- 13. (previously presented) A method of fabricating a semiconductor structure, the method comprising: forming a silicon seed layer over a surface of a substrate; providing openings in the seed layer; selectively forming amorphous silicon over the substrate; and forming monocrystalline SiGe.
- 14. (previously presented) A method as recited in claim 13, further comprising, removing said amorphous silicon in regions where said monocrystalline SiGe is formed.
- 15. (previously presented) A method as recited in claim 14, wherein said removing said amorphous silicon exposes a top surface of the substrate.
- 16. (previously presented) A method as recited in claim 15, wherein the top surface is monocrystalline silicon.
- 17. (previously presented) A method as recited in claim 13, wherein the semiconductor structure includes a lateral pnp transistor.
- 18. (previously presented) A method as recited in claim 13, wherein the semiconductor structure includes a SiGe bipolar transistor.
- 19. (previously presented) A method as recited in claim 13, wherein the semiconductor structure includes a varactor diode.
- 20. (previously presented) A method as recited in claim 13, further comprising forming a polysilicon resistor.